a second set of conductors within a second conductive layer formed above the first insulating layer; and

a second insulating layer formed over the second set of conductors, the second insulating layer having at least one semiconductor element and the second set of conductors imbedded therein;

Cont'd C2

wherein one or more of the first set of conductors and one or more of the second set of conductors are electrically connected to the at least one semiconductor element imbedded in the first insulating layer and the at least one semiconductor element imbedded in the second insulating layer.

REMARKS

Claims 1-6 and 14-17 are pending and under consideration. Claims 1 and 14-17 have been amended. No new matter is being entered, and reconsideration of the claims is respectfully requested.

REJECTION UNDER 35 U.S.C. 103

Claims 1-6 were rejected under 35 U.S.C. 103(a) as being unpatentable over Akram et al. (US 6,235,554) in view of Itabashi et al. (US 6,300, 244). This rejection is respectfully traversed for the reasons stated below.

At pages 2-3 of the Office Action, the Examiner alleges that Akram et al. teaches a semiconductor device comprising "plural pairs of conductor layers 26 having wiring patterns and an insulating layer 46 located thereon...; wherein: a semiconductor element 14 is imbedded inside the insulating layer (See FIG. 1)."

Applicant respectfully submits that contrary to the assertions by the Examiner, Akram et al. at FIGS. 1-4, as relied upon by the Examiner, is limited to two separate insulating layers 44 and 46, wherein the first insulating layer 44 contains a semiconductor element 14 while the second separate insulating layer 46 contains conductors 26 and wires 22. Accordingly, it is respectfully submitted that Akram et al. does not teach or suggest, among other things, a semiconductor device comprising "plural pairs of conductor layers, each pair of conductor layers having wiring patterns and contained within an insulating layer; wherein: a semiconductor element is imbedded inside each said insulating layer," as recited in independent claim 1 of applicant's invention.

Regarding Itabashi et al., it is respectfully submitted that since this patent is relied upon by the Examiner for the limited purpose of illustrating "electrically connecting a wiring pattern to a semiconductor element by flip flop chip mounting and via an anisotropic conductive film," and does not teach or suggest the features of independent claim 1, as pointed out above, which are also lacking in Akram et al., independent claim 1 is patentable over Akram et al. and Itabashi et al., separately, or in combination thereof. Further, for at least the reason that claims 2-6 depend from allowable independent claim 1, these claims are also allowable. Accordingly, withdrawal of this rejection and allowance of these claims are earnestly solicited.

REJECTION UNDER 35 U.S.C. 102

Claims 14-17 were rejected under 35 U.S.C. 102(e) as being anticipated by Akram et al. (US 6,235,554). This rejection is respectfully traversed for the reasons stated below.

Accordingly, it is respectfully submitted that Akram et al. does not each or suggest, among other things, "a first insulating layer; a first conductive layer having wiring patterns and formed within the first insulating layer.; and at least one semiconductor element imbedded within the first insulating layer such that the at least one semiconductor element is electrically connected to at least one of the wiring patterns of the first conductive layer and at least one of the wiring patterns of the second conductive layer," as recited in independent claim 14, as amended. Further, it is respectfully submitted that Akram et al. does not each or suggest, among other things, "a first set of conductors within a first conductive layer; a first insulating layer formed over the first set of conductors, the first insulating layer having at least one semiconductor element and the first set of conductors imbedded therein," as recited in independent claim 17 of applicant's invention, as amended. Accordingly, it is respectfully

submitted that independent claims 14 and 17 are patentable over Akram et al., and withdrawal of this rejection and allowance of these claims are earnestly solicited. Further, for at least the reason that claims 15-16 depend from allowable independent claim 14, it is submitted that these claims are also allowable.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: March 19, 2003

By: _____
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please AMEND the following claims:

1. (TWICE AMENDED) A semiconductor device comprising:

plural pairs of conductor layers, each pair of conductor layers having wiring patterns and being contained within an insulating layer, [located thereon;] wherein:

a semiconductor element is imbedded inside each said insulating layer;

[the] each semiconductor element is electrically connected to a wiring pattern of [said] a respective pair of conductor [layer] layers within the respective insulating layer; and

[a] the wiring pattern of [said] each pair of conductor [layer] layers is electrically connected, by via holes, to a wiring pattern of [the] a conductor layer of a different pair of ~~[a conductor layer]~~ conductor layers having wiring patterns and [an] contained within another insulating layer [located thereon].

14. (ONCE AMENDED) A semiconductor device comprising:

a first insulating layer;

a first conductive layer having wiring patterns and formed [under] within the first insulating layer;

a second conductive layer having wiring patterns and formed over the first insulating layer, one or more of the wiring patterns of the second conductive layer being electrically connected to one or more of the wiring patterns of the first conductive layer through via holes; and

at least one semiconductor element imbedded [inside] within the first insulating layer [and] such that the at least one semiconductor element is electrically connected to at least one of the wiring patterns of the first conductive layer and at least one of the wiring patterns of the second conductive layer.

15. (ONCE AMENDED) The semiconductor device according to claim 14, further comprising a second insulating layer having at least one semiconductor element imbedded

therein, the second insulating layer [being separated from] provided on the first insulating layer [by one of the first and] and containing therein the second [conductor layers] conductive layer, and the at least one semiconductor element of the second insulating layer being electrically connected to one or more of the wiring patterns of the first and second [conductor] conductive layers.

16. (ONCE AMENDED) The semiconductor device according to claim 14, wherein one or more of the wiring patterns of the first [conductor] conductive layer are electrically connected to one or more of the wiring patterns of the second [conductor] conductive layer.

17. (ONCE AMENDED) A semiconductor device comprising:

a substrate;

a first set of conductors within a first conductive layer;

a first insulating layer formed over [a] the first set of [conductor layer] conductors, the first insulating layer having at least one semiconductor element and the first set of conductors imbedded therein [and the first conductor layer having wiring patterns therein];

a second set of conductors within a second conductive layer formed above the first insulating layer; and

a second insulating layer formed over [a] the second set of [conductor layer] conductors, [the second insulating layer and conductor layer being formed over the first insulating layer and first conductor layer,] the second insulating layer having at least one semiconductor element and the second set of conductors imbedded therein [and the second conductor layer having wiring patterns therein];

wherein one or more of the [wiring patterns of the] first set of [conductor layer] conductors and one or more of the second set of [conductor layer] conductors are electrically connected to the at least one semiconductor element imbedded in the first insulating layer and the at least one semiconductor element imbedded in the second insulating layer.